UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,857	06/07/2005	Assaf Shappir		7211

56639 7590 07/10/2008

EMPK & Shiloh, LLP
116 JOHN ST,
SUITE 1201
NEW YORK, NY 10038

EXAMINER	
NGUYEN, DANG T	
ART UNIT	PAPER NUMBER
2824	

MAIL DATE	DELIVERY MODE
07/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/537,857	SHAPPIR ET AL.	
	Examiner	Art Unit	
	DANG T. NGUYEN	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2008 of Applicant's amendments*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to communication filed on 4/28/08. Claims 1, 3, 9, 11 and 19 have been amended.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 6, 9 – 16, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Roohparvar, U.S. Patent No. 6,529,417 – filed: Mar. 29, 2001.

Regarding independent claim 1, Fig. 2 of Roohparvar discloses a method of erasing (222; Col. 4 lines 56 - 58) one or more non-volatile memory cells (202) comprising: applying (222; Col. 4 lines 56 - 58) to the one or more NVM cells (202) an erase pulse (Col. 4 Lines 56 – 58) having a predominantly non-flat voltage profile (Col. 4 line 66 – Col. 5 line 3; also See Fig. 5 [Verase] *for disclosing erase pulse Verase having predominant ramp profile*).

Regarding dependent claim 2, Fig. 5 of Roohparvar further discloses the method according to claim 1, wherein the voltage profile of the erase pulse (Verase) is predefined (Verase profile is predefined as a ramp pulse; See Col. 4 line 66 – Col. 5 line 3).

Regarding dependent claim 3, Fig. 5 of Roohpavar further discloses the method according to claim 2, wherein the erase pulse (Verase) has a voltage profile selected from the group consisting of ramp-like, exponential-growth –like, asymptote-like and stepped (Col. 5 lines 16 – 19 disclosed voltage erase Verase ramped profile).

Regarding dependent claim 4, Fig. 5 of Roohparvar further discloses the method according to claim 3, wherein the erase pulse (Verase) is applied to each sub-set of the set of NVM cells (Fig. 2 [202]) in a staggered sequence (Col. 7 lines 34 - 37).

Regarding dependent claim 5, Fig. 3B of Roohparvar further disclose the method according to claim 1, wherein the voltage profile of the erase pulse (Verase) is dynamically adjusted (Col. 5 line 66 Col. 6 line 10) based on the feedback (313; Col 5 lines 57 – 65).

Regarding dependent claim 6, Fig. 3B further discloses the method according to claim 5, wherein the feedback (Col. 5 lines 60 – 61) comes from a sensor (332) from the group consisting of a current sensor, a voltage sensor, a current derivative sensor, and a voltage derivative sensor (332; see Col 5 lines 57 – 65 discloses Voltage divider network 332 to sense the output (Verase 343) and provided feedback Voltage at the node 304).

Regarding independent claim 9, Fig. 2 of Roohparvar discloses a circuit (222 for erasing (Col. 4 lines 56 - 58) one or non-volatile memory cells (202) comprising, an erase pulse source (222; Col. 4 lines 56 - 58) to produce an erase pulse (Col. 4 Lines 56 – 58) having a non-flat voltage profile (Col. 4 line 66 – Col. 5 line 3; also See Fig. 5 [Verase] *for disclosing erase pulse Verase having ramp profile*).

Regarding dependent claim 10, Roohparvar further discloses the circuit according to claim 9, wherein said erase pulse source comprises a charge-pump (Col. 6 lines 24 - 25).

Regarding dependent claim 11, Fig. 5 of Roohparvare discloses the ciruit according to claim 10, wherein the erase pulse (Verase) has a voltage profile selected from the group consisting of ramp-like, exponential-growth –like, asymptote-like and stepped (Col. 5 lines 16 – 19 *discloses voltage erase Verase ramped profile*)

Regarding dependent claim 12, Fig. 2 of Roohparvar further discloses the circuit according to claim 9, further comprising a cell select circuit (204, 206; Col. 4 lines 45 - 47) adapted to select to which cells of a set of NVM cells (202) the erase pulse (Verase from 222) is applied.

Regarding dependent claim 13, Fig. 2 of Roohparvar discloses the circuit according to claim 12, wherein said cell select circuit (204, 206; (Col. 4 lines 45 - 47)) is adapted to apply the erase pulse (Verase from 222) to each sub-set of the set of NVM cells (202) in a staggered sequence (Col. 7 lines 34 - 37).

Regarding dependent claim 14, Fig. 3B of Roohparvar further discloses the circuit according to claim 9, further comprising a sensor (332) to sense a characteristic (332; Col 5 lines 57 – 65 *discloses Voltage divider network 332 to sense the output 334 Verase and provided feedback Voltage at the node 304*) of the erase pulse (Verase) as it is being applied to the one or more NVM cells (Fig. 2[202]).

Regarding dependent claim 15, Fig. 3B of Roohparvar further discloses the circuit according to claim 14, wherein the sensor (332) is selected from the group

consisting of a current sensor, a voltage sensor, a current derivative sensor, and a voltage derivative sensor (332; Col 5 lines 57 – 65 *discloses Voltage divider network 332 to sense the output 334 Verase and provided feedback Voltage at the node 304*).

Regarding dependent claim 16, Fig. 3B of Roohpavar discloses the circuit according to claim 9, further comprising a controller (350, 330) to cause the erase pulse source (222) to adjust (Col. 5 line 66 Col. 6 line 10) the voltage profile of the erase pulse (Verase) based on a signal (304) from said sensor (332; see Col 5 lines 57 – 65 *discloses Voltage divider network 332 to sense the output Verase 343 and provided feedback Voltage at the node 304*).

Regarding independent claim 19, Fig. 2a of Roohparvar discloses a system for erasing (222; Col. 4 lines 56 - 58) one or non-volatile memory (202) cells comprising: A NVM array (202), and an erase pulse source (222; Col. 4 lines 56 - 58) to produce an erase pulse (222; Col. 4 lines 56 - 58) having a predominantly non-flat voltage profile (Col. 4 line 66 – Col. 5 line 3; also See Fig. 5 [Verase] *for disclosing erase pulse Verase having predominant ramp profile*).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 8, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roohparvar as applied to claims 6 and 16 above, and in view of Chindalore et al., U.S. Patent No. 6,839,280 B1 – filed: Jun. 27, 2003.

Fig. 3B of Roohparvar as applied to claims 6 and 16 above does not disclose wherein the voltage of the erase pulse (Verase) is adjusted in an inversion relation to the current measure by the current sensor, and wherein the voltage of the erase pulse (Verase) is adjusted at a rate correlated to a signal produced by the current derivative sensor.

Fig. 4 of Chindalore et al. disclose the method and circuit according to claims 6 and 16, wherein the voltage of the erase pulse (Vcell) is adjusted in an inversion relation to the current measure by the current sensor (Col. 5 lines 1 – 7 of Chindalore et al. *disclose current feedback sensor device 48 having voltage adjustment, which inversed relation with feedback current decreasing reference current, resulting cell voltage increases over time as the memory is erased*); and wherein the voltage of the erase pulse is adjusted at a rate correlated to a signal produced by the current derivative sensor (Col. 5 lines 1 – 7 of Chindalore et al. also *disclose current feedback sensor device 48 having voltage adjustment correlated to increase or decrease rate of current feedback I REF*).

Roohparvar and Chindalore et al. are common subject matter for erasing non-volatile memory cell. Therefore; it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the concept taught by the voltage profile of Chindalore into the voltage profile of Roohparvar for purpose of

providing adjustment for erase voltage to provide proper erase voltage for the memory cell (Chindalore et al.'s Col. 5 lines 8 – 11).

Response to Arguments

4. Applicant's arguments with respect to amended claims 1, 9, and 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

6. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

7/7/08

/Dang T Nguyen/

Primary Examiner, Art Unit 2824